University of Nevada, Reno

COMPUTER SCIENCE & ENGINEERING DEPARTMENT
CS 219 Computer Organization
Fall 2014

Course Information

- **Credits:** 3.0
- **Lecture hours:** Tuesday & Thursday, 2:30 - 3:45 pm
- **Instructor:** Dwight Egbert, Professor of Computer Science & Engineering (egbert@cse.unr.edu)
- **Office Hours:** 11:30AM-1:00PM Monday & Wednesday (or by appointment); Room 322 SEM; Tel: (775) 784-6952

Description

Introduction to organization and integration of computer components. Topics include: computer abstractions and performance, arithmetic operations, instruction set architecture, assembly programming, datapath, pipelining, memory hierarchy, I/O, and parallel architectures.

Prerequisites

- CS 202 or CPE 201

Textbooks

Required Textbook

- WilliamStallings(2013) Computer Organization and Architecture: Designing for Performance, 9th Edition. Pearson. (ISBN: 0-13-293633-X) - or International Edition (ISBN: 0-273-76919-7) - or CourseSmart eTextbook (ISBN: 0-13-293646-1)

Recommended Reference

- M. M. Mano and C. R. Kime. (2008) Logic and Computer Design Fundamentals, 4th Edition. Pearson. (ISBN: 0-13-600158-0).

Textbook Chapters and Topics — Approximate Calendar

CHAPTER 1 INTRODUCTION — Week 1
1.1 Organization and Architecture
1.2 Structure and Function

CHAPTER 2 COMPUTER EVOLUTION AND PERFORMANCE
2.1 A Brief History of Computers
2.2 Designing for Performance
2.3 Multicore, MICs, and GPGPUs
2.4 The Evolution of the Intel x86 Architecture
2.5 Embedded Systems and the ARM
2.6 Performance Assessment

CHAPTER 3 A TOP-LEVEL VIEW OF
COMPUTER FUNCTION AND INTERCONNECTION — Week 2
3.1 Computer Components
3.2 Computer Function
3.3 Interconnection Structures
3.4 Bus Interconnection

3.5 Point-to-Point Interconnect
3.6 PCI Express

CHAPTER 11 DIGITAL LOGIC
11.1 Boolean Algebra

CHAPTER 10 NUMBER SYSTEMS — Week 3
9.1 The Decimal System
9.2 Positional Number Systems
9.3 The Binary System
9.4 Converting Between Binary and Decimal
9.5 Hexadecimal Notation

CHAPTER 10 COMPUTER ARITHMETIC
10.1 The Arithmetic and Logic Unit
10.2 Integer Representation
10.3 Integer Arithmetic
10.4 Floating-Point Representation
10.5 Floating-Point Arithmetic

CHAPTER 12 INSTRUCTION SETS: CHARACTERISTICS AND FUNCTIONS — Week 4
12.1 Machine Instruction Characteristics
12.2 Types of Operands
12.3 Intel x86 and ARM Data Types
12.4 Types of Operations
12.5 Intel x86 and ARM Operation Types
Appendix 12A Little-, Big-, and Bi-Endian

CHAPTER 13 INSTRUCTION SETS: ADDRESSING MODES AND FORMATS — Week 5
13.1 Addressing Modes
13.2 x86 and ARM Addressing Modes
13.3 Instruction Formats
13.4 x86 and ARM Instruction Formats
13.5 Assembly Language

CHAPTER 14 PROCESSOR STRUCTURE AND FUNCTION — Week 6
14.1 Processor Organization
14.2 Register Organization
14.3 Instruction Cycle
14.4 Instruction Pipelining
14.5 The x86 Processor Family
14.6 The Arm Processor

APPENDIX B ASSEMBLY LANGUAGE AND RELATED TOPICS — Weeks 7 - 9
B.1 Assembly Language
B.2 Assemblers
B.3 Loading and Linking — MidTerm Exam - date TBA

CHAPTER 15 REDUCED INSTRUCTION SET COMPUTERS
15.1 Instruction Execution Characteristics
15.2 The Use of a Large Register File
15.3 Compiler-Based Register Optimization
15.4 Reduced Instruction Set Architecture
15.5 RISC Pipelining
15.6 MIPS R4000
15.7 SPARC
15.8 RISC versus CISC Controversy

CHAPTER 4 CACHE MEMORY — Week 10
4.1 Computer Memory System Overview
4.2 Cache Memory Principles

4.3 Elements of Cache Design
4.4 Pentium 4 Cache Organization
4.5 ARM Cache Organization

CHAPTER 5 INTERNAL MEMORY — Week 11
5.1 Semiconductor Main Memory
5.2 Error Correction
5.3 Advanced DRAM Organization

CHAPTER 6 EXTERNAL MEMORY
6.1 Magnetic Disk
6.2 RAID
6.3 Solid State Drives
6.4 Optical Memory
6.5 Magnetic Tape

CHAPTER 7 INPUT/OUTPUT — Week 12
7.1 External Devices
7.2 I/O Modules
7.3 Programmed I/O
7.4 Interrupt-Driven I/O
7.5 Direct Memory Access
7.6 I/O Channels and Processors
7.7 The External Interface: Thunderbolt and InfiniBand
7.8 IBM zEnterprise 196 I/O Structure

CHAPTER 8 OPERATING SYSTEM SUPPORT — Week 13
8.1 Operating System Overview
8.2 Scheduling
8.4 Pentium Memory Management
8.5 ARM Memory Management

CHAPTER 16 INSTRUCTION-LEVEL PARALLELISM
AND SUPERSCALAR PROCESSORS
16.1 Overview
16.2 Design Issues
16.3 Pentium 4
16.4 ARM Cortex-A8

CHAPTER 17 PARALLEL PROCESSING — Week 14
17.1 Multiple Processor Organizations
17.2 Symmetric Multiprocessors
17.3 Cache Coherence and the MESI Protocol
17.4 Multithreading and Chip Multiprocessors
17.5 Clusters
17.6 Nonuniform Memory Access
17.7 Vector Computation

CHAPTER 18 MULTICORE COMPUTERS
18.1 Hardware Performance Issues
18.2 Software Performance Issues
18.3 Multicore Organization
18.4 Intel x86 Multicore Organization
18.5 ARM11 MPCore
18.6 IBM zEnterprise 196 Mainframe

Review — **Week 15 Final Exam**

Student Participation

- **Disability Statement** If you have a disability for which you will need to request accommodations, please contact the instructor or someone at the Disability Resource Center (Thompson Student Services - 107) as soon as possible.
- **Important Policy** Surreptitious or covert videotaping of class or unauthorized audio recording of class is prohibited by law and by Board of Regents policy. This class may be videotaped or audio recorded only with the written permission of the instructor. In order to accommodate students with disabilities, some students may have been given permission to record class lectures and discussions. Therefore, students should understand that their comments during class may be recorded.
- **Academic Success Services** Your student fees cover usage of the Math Center (784-4433 or www.unr.edu/mathcenter/), Tutoring Center (784-6801 or www.unr.edu/tutoring/), and University Writing Center (784-6030 or www.unr.edu/writing_center/. These centers support your classroom learning; it is your responsibility to take advantage of their services. Keep in mind that seeking help outside of class is the sign of a responsible and successful student.

The course will contain two basic and interrelated blocks. First, the textbook will provide the framework for the course. Second, as material is reached in the textbook it will be related to supplementary material covering advanced computer topics.

Students are expected to attend all classes and read all of the assigned sections of the textbook. Often, material will not be covered in both lectures and reading assignments. Thus, both are essential to a full understanding of the course content. During most classes a short example problem related to the current topic will be assigned. Students will spend a few minutes working alone on this problem followed by a few minutes discussing their solutions with two or three other students. These solutions will be collected and used as a basis for up to 5% extra credit for the course grade.

Also, completion of homework is essential. **Homework will be due each TUESDAY**, or the next following class if there is no Tuesday class.

LATE HOMEWORK WILL BE ACCEPTED FOR AT MOST 50% CREDIT.

Students are encouraged to study together, but each person must prepare his or her solutions and have a firm understanding of any work turned in. When you put your name on your homework you are stating that it is your own work and not the work of another person. As a reminder of UNR academic standards, please read from the ***UNR on-line Catalog, University Code of Conduct and Policies, POLICIES AND GUIDELINES, ACADEMIC STANDARDS*** http://www.cis.unr.edu/ecatalog/Default.aspx?article_list_id=29351 defining these standards. Specifically, the following: "*Plagiarism is defined as submitting the language, ideas, thoughts or work of another as one's own; or assisting in the act of plagiarism by allowing one's work to be used in this fashion*." This means that if another student asks to borrow your work to copy - JUST SAY NO - or you are participating in plagiarism.

Course Grade Structure

Each course activity will contribute to the course grade as shown below. All activities will be graded on a scale of 0-100 points, and the final course grade will be determined as shown below.

Students must have an average score for both exams of 50 or greater in order to pass the course

All exams given in this course will be closed notes and closed books. Only calculators and materials handed out at the time of the exam may be used. Normally, plus/minus grades are not given in this class. The instructor reserves the right to assign plus/minus grades under special circumstances involving borderline grades based upon class participation. Your grade will never be lower than defined here unless you have an excessive number of un-excused absences from class, however, positive class participation can be used as a basis for raising your grade.

HOMEWORK	30%
MID TERM EXAM	30%
COMPREHENSIVE FINAL EXAM	40%
= COURSE GRADE	100%

90 - 100 points = A | 80 - 89.9 points = B | 65 - 79.9 points = C | 50 - 64.9 points = D | 00 - 49.9 points = F

Learning Outcomes:

Learning Outcome A: Students will be able to describe the structure and functioning of a digital computer, including its overall system architecture, operating system, and digital components.

Learning Outcome B: Students will be able to explain the generic principles that underlie the building of a digital computer, including data representation, digital logic and processor programming.

Learning Outcome C: Students will be able to apply some fundamental coding schemes.

Learning Outcome D: Students will be able to present and discuss simple examples of assembly language appropriate for an introductory course.

Course Outcomes:

The course outcomes are skills and abilities students should have acquired by the end of the course. These outcomes are defined in terms of the Computer Science and Engineering ABET Accreditation Program outcomes which are relevant to this course. All outcomes are listed below and those relevant to this course are identified in the following Table.

1. an ability to apply knowledge of computing, mathematics, science, and engineering.
2. an ability to design and conduct experiments, as well as to analyze and interpret data.
3. an ability to design, implement, and evaluate a computer-based system, process, component, or program to meet desired needs, within realistic constraints specific to the field.
4. an ability to function effectively on multi-disciplinary teams.
5. an ability to analyze a problem, and identify, formulate and use the appropriate computing and engineering requirements for obtaining its solution.
6. an understanding of professional, ethical, legal, security and social issues and responsibilities.
7. an ability to communicate effectively with a range of audiences.
8. the broad education necessary to analyze the local and global impact of computing and engineering solutions on individuals, organizations, and society.
9. a recognition of the need for, and an ability to engage in continuing professional development and life-long learning.
10. a knowledge of contemporary issues.
11. an ability to use current techniques, skills, and tools necessary for computing and engineering practice.
12. an ability to apply mathematical foundations, algorithmic principles, and computer science and engineering theory in the modeling and design of computer-based systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.
13. an ability to apply design and development principles in the construction of software systems or computer systems of varying complexity.

Program Outcomes	Course Outcomes	Course Strategies & Actions
3	Students demonstrate that they understand the building blocks of modern computers, including the feature trade-offs involved with different modern architectures.	Study of both Princeton and Harvard Architectures. Examination of components within the CPU. Homework and exam questions covering these topics.
9	Students demonstrate that they understand how computer architectures change and evolve as the technology and market change.	Study of how different CPU features support different computer applications. Homework requiring Web searches for details of current implementations.
10	Students demonstrate that they can learn the assembly language for more than a single CPU architecture.	Homework requiring specific program functions. Examination of assembly language for both Intel 8086 CISC and ARM 7 RISC processors.