CPE 201 – Introduction to Computer Engineering

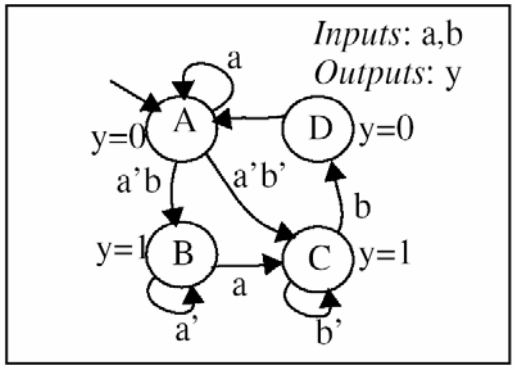
Fall 2007

Homework 5

Due date: November 27, 2007

1. [10 points] Draw a state diagram for a sequential circuit with one input I, and three outputs x, y, and z. The output xyz should always follow the following sequence: 000, 001, 010, 100, repeat. The input I stops the sequence whenever is set to 0. When the input I returns to 1, the sequence resumes from where it left off. The initial state is 000.

2. [10 points] Using the five-step process for designing a controller, convert the finite state machine from the figure below to a controller circuit, implementing it using a state register (built with D flip-flops) and logic gates.



3. [10 points] A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations:

$J_A = x$ $K_A = B'$

$J_B = x$ $K_B = A$

(a) [5 points] Derive the state equations A(t+1) and B(t+1) by substituting the input equations for the J and K variables.

(b) [5 points] Draw the state diagram of the circuit.

4. [10 points] Design a 4-bit register with 2 control inputs s1 and s0, 4 data inputs I3, I2, I1 and I0, and 4 data outputs Q3, Q2, Q1 and Q0. When s1s0=00, the register maintains its value. When s1s0=01, the register loads I3..I0. When s1s0=10, the register clears itself to 0000. When

s1s0=11, the register reverses its bits, so 1110 would become 0111 and 1010 would become 0101.

Extra credit:

1. [10 points] Design an 8 bit shifter circuit, that shifts its inputs two bits to the right (shifting in 0s) when the shifter's **shift** control input is 1.