

CPE 201 – Introduction to Computer Engineering

Fall 2007

Homework 6

Due date: December 11, 2007

1. [10 points] Problem 7.1 (page 329).
2. [10 points] Problem 7.11 (page 330). Show all of your work leading to the result.
3. [10 points] Problem 7.12 (page 330). Show all of your work leading to the result.
4. [10 points] Problem 7.23 (page 332).

Extra credit:

1. [10 points] Use the register transfer level (RTL) design method discussed in class to convert the high level state machine from the figure below to a *controller* and *datapath*. Design the controller to an FSM only.

Inputs: start(bit), data(8 bits), addr(8 bits), w_wait(bit)

Outputs: w_data(8 bits), w_addr(8 bits), w_wr(bit)

