
2. [10 points] Problem 7.11 (page 330). Show all of your work leading to the result.

3. [10 points] Problem 7.12 (page 330). Show all of your work leading to the result.

4. [10 points] Problem 7.23 (page 332).

Extra credit:

1. [10 points] Use the register transfer level (RTL) design method discussed in class to convert the high level state machine from the figure below to a controller and datapath. Design the controller to an FSM only.

\[\text{Inputs:}\] start(bit), data(8 bits), addr(8 bits), w_wait(bit)  
\[\text{Outputs:}\] w_data(8 bits), w_addr(8 bits), w_wr(bit)

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**Diagram:**

- State: Wait
  - Input: start
  - Output: w_wait
- State: Start 't
  - Input: w_wait
  - Output: Send Addr
- State: Send Addr
  - Input: w_wr=1, w_addr=addr
- State: Send Data
  - Input: w_data=data
  - Output: w_wait